# Pixel detector of Silicon Vertex Tracker for PHENIX at RHIC

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The Silicon Vertex Tracker(VTX) for the Pioneering High Energy Nuclear Interaction eXperiment(PHENIX) experiment at the Brookhaven National Laboratory(BNL) will be installed into the innermost of PHENIX detector in 2009. The VTX will enhance physics capability of PHENIX. The first readout and cosmic telescope test for pixel with almost actual readout system had achieved successfully in last year, 2006.

## 1. Introduction

The Relativistic Heavy Ion Collider (RHIC) at BNL provides collisions of polarized proton-proton up to $\sqrt{s} = 500$GeV and heavy ion up to $\sqrt{s_{NN}} = 200$GeV. The designed luminosity is $2 \times 10^{32} cm^{-2} s^{-2}$ in the 500GeV proton collisions and the maximum bunch is 120. PHENIX[1] is one of two major experiments at RHIC. The PHENIX detector consists of 2 central arms detecting photons, electrons and hadrons at mid-rapidity and the muon arms detecting muons in forward rapidity.

The VTX[2] will identify heavy quark productions by measuring displaced decay vertices, and will reconstruct jets with large acceptance that covers almost $2\pi$ in the $\phi$ direction and $|\eta| < 1.2$. These measurements provided fundamental information of gluon polarization in polarized proton-proton collision and direct signals from Quark Gluon Plasma(QGP) in heavy ion collision. The VTX consists of two types of detectors; the inner two layers are pixel-type and the outer two layers are strip-type detectors[3]. Fig.2 shows 3D model pictures of the VTX detector.

## 2. Overview of pixel detector

The specifications of the pixel detector are summarized in Table.1. The pixel subsystem is made of 30 ladders, 10 for the first layer and 20 for the 2nd layer surrounding the beam pipe. A pixel ladder consists of two half ladders on a single mechanical support plate including cooling structure. A half ladder is the fundamental electrical read-out unit of the system. It consists of two sensor modules connected by a read-out bus. A sensor module is made of a sensor chip and 4 readout chips. The

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sensors are fabricated by CANBERRA electronique in France[4]. The readout chip, ALICE1LHCb[5], is originally developed by CERN for ALICE and LHCb Silicon Pixel Detector[6].

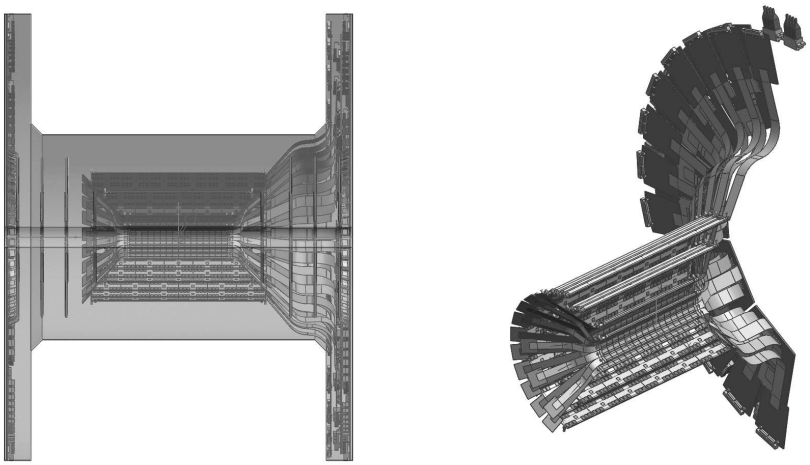

Fig. 1. *Cross section of VTX*

| Sensor type | Pixel | |
|---|---|---|
| Layer | 1 | 2 |
| r(cm) | 2.5 | 5 |
| Channel Size | 50$\mu$m $\times$ 425 $\mu$m | |
| Sensor chip size | 56.72mm$\times$13.92mm$\times$0.2mm | |
| Ladders | 10 | 20 |
| Readout Channel | 1310720 | 2621440 |
| Occupancy at central AuAu@$\sqrt{s} = 200GeV$ | 0.53% | 0.16% |
| X/X0 | 1.44% | |

Table 1. *Specification of PHENIX VTX.*

## 3. Developments of prototype pixel detector components

### 3.1. *Pixel sensor module*

A sensor module consists of a pixel sensor chip and 4 ALICE1LHCb readout chips. A pixel sensor chip has 4 arrays of 32 by 256 pixels of 50$\mu$m $\times$ 425$\mu$m size and each array is read out by a single read-out chip. ALICE1LHCb chip is designed in a 0.25$\mu$m CMOS process at IBM with radiation tolerant design layout techniques.

Each chip has 32 by 256 signal processing units of 50$\mu$m $\times$ 425$\mu$m so that the size and the pitch of the processing unit match those of the pixels on the sensor. Four chips are bump bonded on a pixel sensor by VTT in Finland to form a sensor module.

A block diagram of a signal processing unit in the ALICE1LHCb chip is shown in Fig.2. Analog signals from a pixel are pre-amplified and are discriminated to binary ON/OFF data of the pixel. The data are sent to a digital delay unit to wait for the level-1 trigger decision. Once the event is triggered, the data are stored into a 4 events deep FIFO buffer to be read out by a down stream data acquisition system. The data are also sent to the Fast-OR self trigger logic unit of the chip. All configurations are set via the JTAG serial interface. The maximum readout speed is 100nsec$\times$256= 25.6$\mu$sec/chip with a 32-bit when the chip is operated at 10 MHz.

A typical full depletion voltage of pixel sensors is 50V. Minimum Ionizing Particle(MIP) deposits about 53KeV of energy in the sensor, producing approximately 14000 electron-hole pairs. Electrical noise of readout chip is measured as $\sim$120 electrons equivalent. It means signal to noise ratio $\sim$120.

Extensive Q/A tests of the read-out chips are performed at CERN and RIKEN to select fully functional chips. Those tests includes..... Selected chips confirmed to be fully functional are sent for VTT and bump bonded.

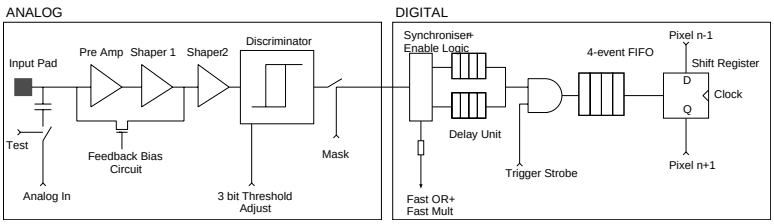


Fig. 2. *Block diagram of processing unit in a pixel of ALICE1LHCb.*

### 3.2. *Pixel bus*

A pixel bus is a fine pitch, multi-layer, flexible printed circuit board for data readout and control which connects two sensor modules and a Silicon Pixel Interface Read Out(SPIRO) module. Two types of bus, 3cm width bus and 1.5cm width bus, were developed by RIKEN. The former is 1st prototype was developed to verify readout test existing technology of industry standard Cu-polyimide bus. The size is 3.0cm$\times$25cm stacked 5 layers circuit. The latter is 2nd prototype almost same design for actual experiment. The size is 1.5cm$\times$25cm stacked 6 layers circuit. 1.5cm bus is adopted new technology, Cu-Al-polyimide bus, to reduce radiation length because Al is about 1/6 radiation length of Cu.

A SPICE[7] simulator is used to evaluate the bus performances of pulse propa-

gation, impedance and crosstalk. In this simulation, the bus length is 25cm, signal lines are 70 $\mu$m wide with a 50 $\mu$m space, and polyimide films among the layers are 50 $\mu$m thick. We also measured performance of the prototype bus. The pulse shape at its terminal satisfy the requirement of GTL-level[8] operation. The maximum crosstalk of adjacent lines is 0.3V which is attenuated quickly and far from GTL H/L logic threshold.

### 3.3. *SPIRO*

Readout and control of 4×2 readout chips are performed by SPIRO board. It is implemented 2 digital pilot ASICs, 2 analog pilot ASICs, 2 Giga-bit Optical Link(GOL) ASICs and a FPGA into a board. SPIRO boards will be located at near the beam collision point so that each component have a sufficient radiation tolerance. Digital pilot ASIC plays a role of readout by multiplexing and control of readout chips, supplying 40MHz clock and serial control signal from Front End Module(FEM) at far from experimental hall. 32 column × 256 row pixel in a readout chip was read out every two chips as a unit to column direction in Fig.3. Analog pilot ASIC supplies reference voltage to control threshold for readout chip. GOL serialize and transfer data as a Ethernet by 8b/10b protocol at 1.6Gbps speed. Digital pilot ASIC have been modified based on the ALICE chip architecture, which has an extended data bus width (32-bit to 64-bit) for PHENIX.

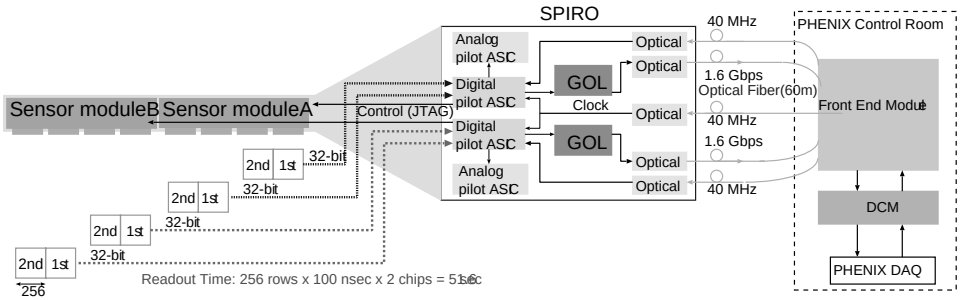


Fig. 3. Readout data

### 3.4. *Assembly*

We need to assemble total forty pixel ladders( 30+10 spare ). These must be supplied efficiently from viewpoint of time and cost at production phase. Furthermore, four pixel sensor modules in each assembled ladders must be kept under $10\mu m$ position alignment from physics requirement. We developed several special fixtures for pixel ladder assembly in spring 2006.

The assembly bench in Fig.4 has a microscope camera with 20× magnification to observe alignment mark on the sensor module by monitor, and also has a long

stroke stage which keep under 10 $\mu m$ precision in the running range. The stage have a magnetometer which measure its position in sub-$\mu m$ level precision. Some special fixtures for specific usage are set to the assembly bench or adhesive dispenser robot stage in Fig.5; Alignment for 4 sensor modules and pickup aligned 4 sensors procedures are performed on the assembly bench. Dispensing adhesive and gluing 4 sensor modules and support procedures are performed on the dispenser robot stage. Also, alignment parameters for each ladders will be measured with 3D measurement machine after assembly and they are inputed the software to get for required resolution as a whole VTX detector.

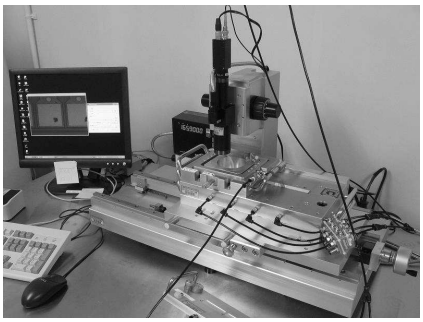

Fig. 4. Assembly bench

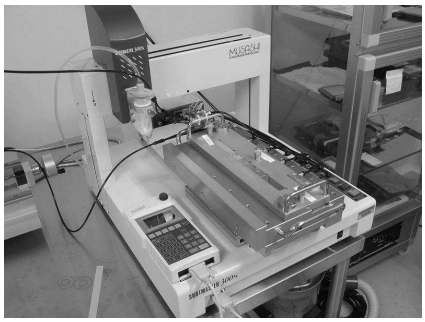

Fig. 5. *Adhesive dispenser robot.*

Requirements for adhesive used to glue between 4 sensors and support and 2 buses are; radiation hardness, long term stability, curing room temperature and good thermal conductance but electric insulator. Araldite 2011 which is known as radiation hard adhesive is chose to satisfy the requirements. We have been tested dispensing the adhesive with varying parameters, such as temperature, curing time, dispensing pressure and needle. Now, we understood the optimization of parameters. Procedure for assembly at production phase have been developing steadily. Production of pixel ladder with the special fixtures will start at summer 2007.

## 4. Cosmic telescope test

Three prototype pixel half-ladders were assembled by craftsman of Hayashi Seimitsu Co. in Japan. Cosmic telescope test with the three half-ladders and readout electronics combined with together had been tested at Stony Brook University on summer 2006. The setup in Fig.6 generated trigger from logical AND circuit of two scintillators and self-trigger of pixel half-ladder. Both individual sub-systems and a unified system are found to work properly. Total 56 cosmic events are taken for 32 hours during 2th to 4th August 2006. Fig7 shows one of the reconstructed cosmic data.

In summary, we had fabricated three prototype pixel detectors with components

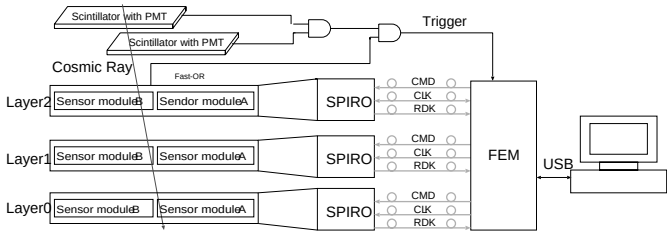


Fig. 6. Cosmic test setup.

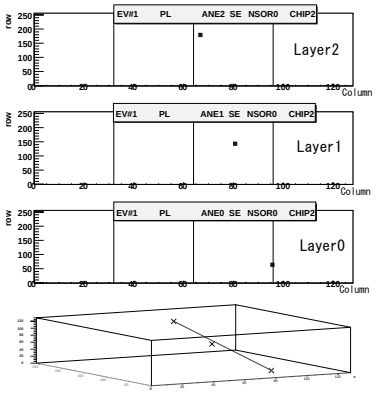


Fig. 7. Reconstructed cosmic event.

used actual experiment and combined into the cosmic telescope. The telescope demonstrates to work properly both hardware and software.

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